Low-Depth, Low-Size Circuits for Cryptographic Applications

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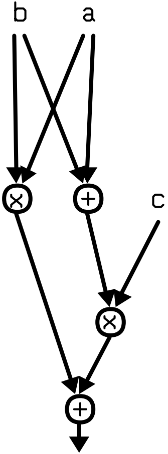
BFA 2017

Circuits over $GF(2)$

AND gates $\times / \wedge$ XOR gates $+$ XNOR gates $\#$



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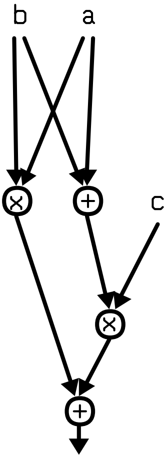

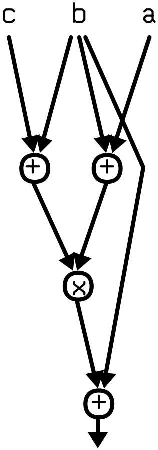

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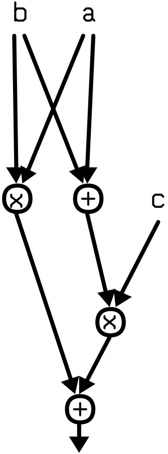

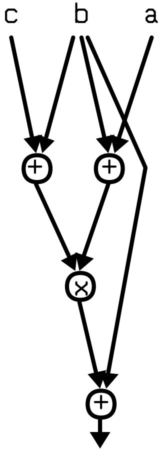

Both circuits compute the *predicate* MAJ(a,b,c) in *size* 4 and *depth* 3.

Boolean Circuit Complexity

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SDU

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- Shannon-Lupanov bound: the circuit complexity of a predicate on n bits is about $\frac{2^n}{n}$ almost everywhere.

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- Almost all Boolean predicates on n bits have multiplicative complexity close to $2^{\frac{n}{2}}$ (i.e. about the square root of the total number of gates needed). [B., Peralta, Pochuev],[Nechiporuk]
- Our thesis is that this observation can be used for Boolean circuit optimization.

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2. Multi-party computations:
   Communication complexity can depend (only) on the number of ANDs in the circuit.
3. Homomorphic computations:
   Performing computations on encrypted data, such as in the cloud.
   The multiplicative complexity can affect the number of bootstrappings.

An example function: AES S-Box

Advanced Encryption Standard (AES)

Block cipher - 128 bit blocks, 128 bit keys

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Block cipher - 128 bit blocks, 128 bit keys

10 rounds using 4 operations:

- SubBytes — Nonlinear substitution step (S-Box)
- ShiftRows
- MixColumns
- AddRoundKey

AES S-Box

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Inversion in $GF(2^8)$, followed by affine transformation (linear, followed by some negations).

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Can be done by *table look-up*.

- 256 different inputs, each with 8 bits output
- 2048 bits
- large area — 16 S-Boxes in each round

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Tower of fields constructions:

- Concentration on size:
  - Wolkerstorfer, Oswald, Lamberger 2002
    — work over subfield $GF(2^4)$
  - Satoh, Morioka, Takano, Munetoh 2001
    — within $GF(2^4)$ use $GF(2^2)$
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    depth 28

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- Depth:
  - Canright 2005 — depth 25 ($\geq$ 125 gates)
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    - depth 22, size 148

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    - depth 22, size 148
  - B., Peralta 2012 — depth 16, size 128
  - this presentation — depth 16, size 125, more automated

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Goal: minimize size (number of gates) and depth

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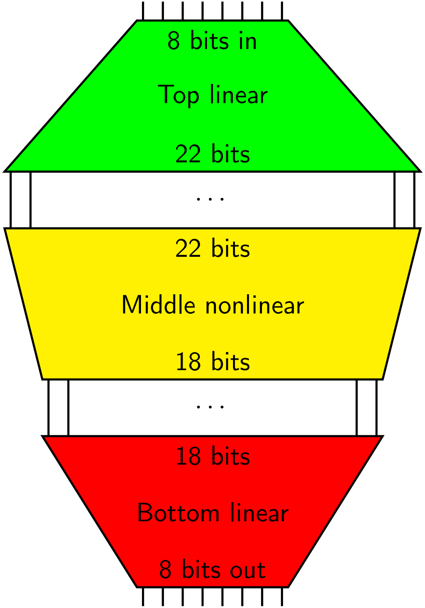
2. Use techniques from automatic theorem proving to re-synthesize non-linear components into lower-depth constructions
   (reused from [B., Peralta 2012])
3. Apply a randomized, greedy heuristic to re-synthesize linear components into lower-depth constructions, using a new
   See-Saw Method

Circuit for the S-Box of AES



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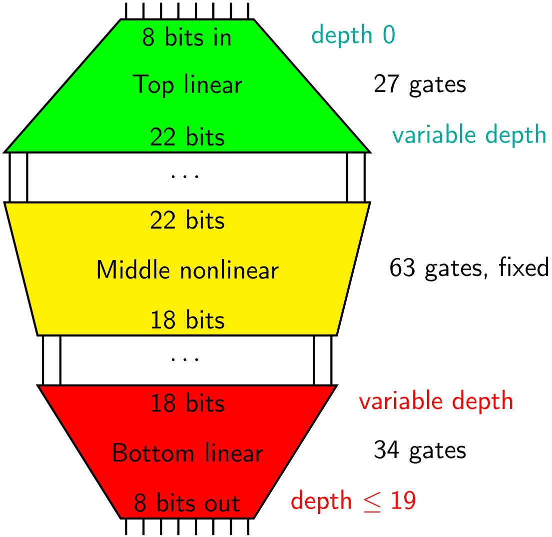

Start: Total depth 19, size 124 gates.

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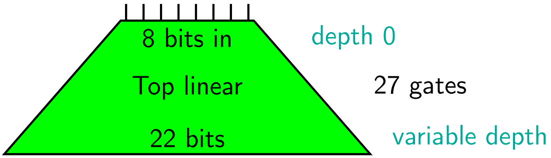
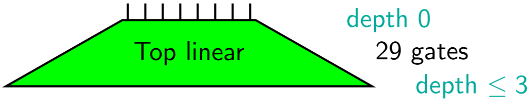


After processing....



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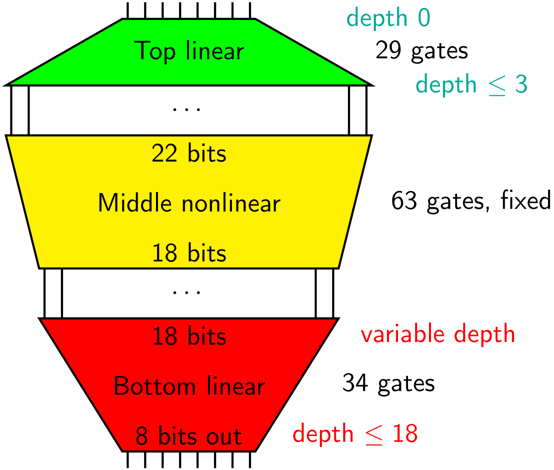

Start: Total depth 19, size 124 gates.
Now: Total depth 18, size 126 gates.

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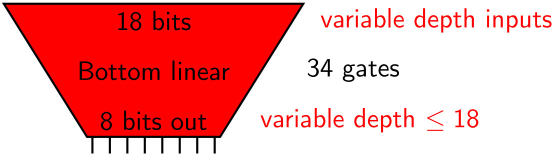

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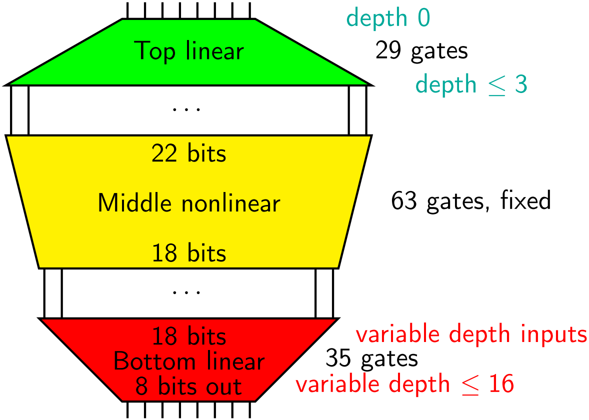

Previous: Total depth 18, size 126 gates.
Now: Total depth 16, size 127 gates.

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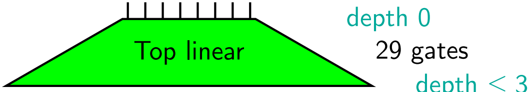

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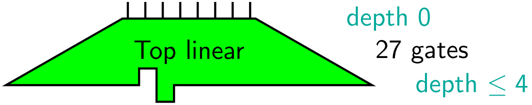

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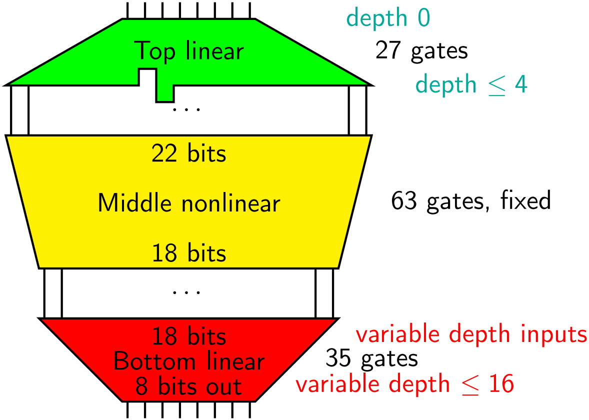

Previous: Total depth 16, size 127 gates.
Now: Total depth 16, size 125 gates.

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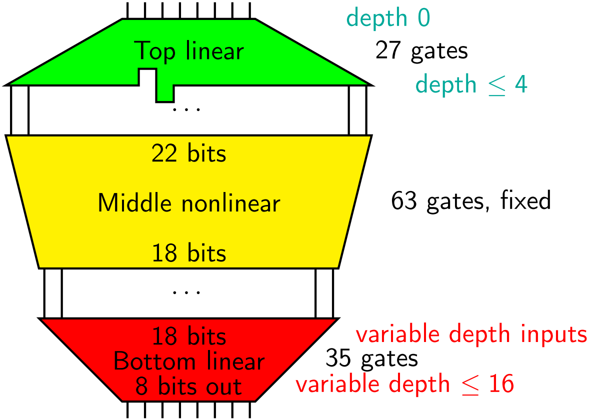

Previous: Total depth 16, size 127 gates.
Now: Total depth 16, size 125 gates.

Work on bottom linear to get all outputs at depth 16.

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Allow some cancellation, using preprocessing.

Other results (polynomial multiplication)

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  Find, Peralta 2016 — 154 gates, and depth 9.
  Using the Find-Peralta nonlinear component, we achieved 154 gates in depth 7.

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- Multiplication of degree 12 polynomials over $GF(2)$:
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  Used in a 16-bit S-box from [Kelly,Kaminsky,Kurdziel,Lukowiak,Radziszowski 2015]
  "Customizable spone-based authenticated encryption using 16-bit S-boxes"
  Reduced 1382 gates to 462.

Thank you for your attention.